EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. David Hardy on 12/16/2009.

2. The application has been amended as follows: The following changes to the drawings have been approved by the examiner and agreed upon by applicant: Add "Related Art" labels to Figures 1-8 and 30. In order to avoid abandonment of the application, applicant must make these above agreed upon drawing changes.

REASONS FOR ALLOWANCE

3. The following is an examiner's statement of reasons for allowance: Referring to **claims 1 and 19**, the prior art of record does not disclose or suggest a device/method comprising a first semiconductor region and a second semiconductor region both comprising semiconductor layers wherein the semiconductor layers of the second semiconductor region are placed "between the semiconductor layers in the first semiconductor region" as recited within the context of the claims. Claims 3-6 and 8-18 are dependent of claim 1, and allowable for the same reasons, while claims 20-24, 26-28 and 30-38 are dependent of claim 19, and allowable for the same reasons.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. More specifically: Park et al. (US 2005/0145932 A1, Fig. 33) as well as Achuthan et al. (US 6,756,643 B1, Figs. 8-10) both disclose a second semiconductor region placed opposing/sandwiching a first semiconductor region, but fail to disclose or suggest placing layers of said second semiconductor region between the layers of said first semiconductor region. In addition, Wu et al. (US 2004/0048424 A1, Figs 11A-11B) discloses placing semiconductor layers, of a second semiconductor region, sandwiching/between semiconductor layers, of a first semiconductor region, but it fails to disclose or suggest a plurality of semiconductor layers of said first semiconductor region to a transistor as well as said second semiconductor region opposing both sides of said first semiconductor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andres Munoz whose telephone number is (571) 270-3346. The examiner can normally be reached on 7:30am - 4:00pm (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andres Munoz/
Examiner, Art Unit 2894
December 16, 2009

/Evan Pert/
Primary Examiner, Art Unit 2826